REMARKS

Claim Rejections - 35 U.S.C. § 103

Claims 30, 32, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,168,072 to Moslehi and US Patent No. 5,124,762 to Childs et al.

The Applicant respectfully traverses. The cited references fail to teach or render obvious, either individually or in combination, all of the elements of the Applicant's claims. In particular, the cited references fail to teach the element of independent claim 30 of "forming a pair of sidewall spacers on opposite sides of the gate electrode and the gate dielectric layer, the sidewall spacers having a spacer height, depositing a metal layer over the sidewall spacers and the gate electrode to a thickness over the gate electrode sufficient to form a silicide having a height less than the spacer height, and forming a silicide layer on the semiconductor material film, the third thickness less than the spacer height to confine the silicide to prevent silicide encroachment." In contrast, Moslehi teaches forming a refractory metal layer 97 over sidewall spacers 60 and gate electrode 88 that has a height over the gate electrode 88 that is far higher than the sidewall spacers 60, as illustrated in Figure 18, and forming a reacted refractory metal interconnect segment 96 over the gate electrode 88 that is not less than the height of the sidewall spacers 60 as illustrated in Figure 19 to prevent silicide encroachment. Childs fails to teach the formation of sidewall spacers, the deposition of a metal layer over sidewall spacers, or the formation of the silicide layer having a thickness less than the height of the spacer height. Therefore, the Applicant respectfully submits that the cited references, either individually or in combination, fail to teach or render obvious each of the elements of independent claim 30 and the claims that depend upon and incorporate the elements of claim 30.

The cited references also fail to teach the element of independent claim 30 of forming a pair of sidewall spacers having a height above the third thickness of the silicide layer on the semiconductor material film on the gate electrode. Also, it would not be obvious to form the sidewall spacers of Demirlioglu or Moslehi to have a height above the third thickness of the silicide layer because neither form a silicide layer as thick as the one claimed by the Applicant to necessitate the formation of sidewall spacers above the height of the thickness of the silicide layer to prevent bridging and shorting of the silicide layer on the gate electrode with the silicide layer on the source and drain regions.

Therefore, the Applicant respectfully submits that the cited references, either in individually or in combination, fail to teach or render obvious claim 30 and claims 32, 36, and 37 that depend upon and incorporate the limitations of independent claim 30.